METHOD FOR FABRICATING A LOW TEMPERATURE POLYSILICON THIN FILM TRANSISTOR

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BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The invention relates in general to a method for fabricating a low temperature polysilicon thin film transistor, and more particularly to a method of fabricating a low temperature polysilicon thin film transistor without residues of photoresist and chemicals.

Description of the Related Art

[0002] Polysilicon and amorphous silicon are two commonly used materials for thin film transistors (TFTs). Low temperature polysilicon TFTs have the advantages of higher electron mobility and drive current over amorphous TFTs. Therefore, the development and improvement of low temperature polysilicon TFTs fabrication process are now of great demand. Within the field of improving the low temperature polysilicon TFTs fabrication

process, residues of photoresist and chemicals during the photolithography and etching process is an important issue.

[0003] Figures 1A to 1J are cross-sectional views showing the sequential process steps of a conventional method for fabricating a low temperature polysilicon thin film transistor. Referring to Figure 1A, a buffer layer 102 is first formed on a substrate 100 and a polysilicon layer 104 is then formed on the buffer layer 102. The polysilicon layer 104 is formed by annealing amorphous silicon, using excimer laser. Next, a patterned photoresist layer 105 is formed on the polysilicon layer 104. The polysilicon layer 104 is etched using the patterned photoresist layer 105 as a mask. The photoresist layer 105 is then removed by using chemicals, such as wet dip. The structure after wet dip is shown in Figure 1B.

[0004] Referring to Figure 1C, a gate oxide layer 108 is formed over the polysilicon layer 104, and a conductive layer is disposed on the gate oxide layer 108. Photolithography and etching processes are then performed to define the gate oxide layer 108 as a patterned gate 110. Next, referring to Figure 1D, a photoresist layer 112 is formed on the gate 110 and on the gate oxide layer 108. Then, a heavily doping process, with high dosage of phosphorus, is performed to form source/drain region 104a, 104b of NMOS device of a CMOS transistor and also form source/drain region 104c, 104d of

a NMOS device in a pixel area.

[0005] The photoresist layer 112 is then removed. Low dosage of phosphorus is then implanted into the substrate 100 to form lightly doped source/drain regions 104m, 104x, 104n and 104y of the NMOS transistor, as shown in Figure 1E. Next, referring to Figure 1F, a photoresist layer 114 is formed on the gate 110 and the gate oxide layer 108. Using the photoresist layer 114 as a mask, high dosage of boron is implanted in the substrate 100 to form source/drain region 104i, 104j of a PMOS transistor.

[0006] Referring to Figure 1G, the photoresist layer 114 is removed. An interlayer dielectric 116 is formed on the gate 110 and on the gate oxide layer 108. There are a number of openings formed within the gate oxide layer 108 and within the interlayer dielectric 116. Then, referring to Figure 1H, electrodes 118 are formed on the interlayer dielectric 116. The electrodes 118 fill the openings within the gate oxide layer 108 and within the interlayer dielectric 116. The electrodes 118 thereby electrically connect the source/drain regions 104a, 104c, 104i, 104b, 104d and 104j.

[0007] Referring to Figure 1I, a passivation layer 120 is formed on the electrodes 118 and the interlayer dielectric 116. An opening is formed through the passivation layer 120 to expose the electrodes 118. Next, a

transparent electrode 122 is formed on the passivation layer 120. The transparent electrode 122 fills the opening within the passivation layer 120 to electrically connect the electrode 118, as shown in Figure 1J. A structure resulting from this process is shown in Figure 1J.

[0008] In the low temperature polysilicon TFT fabricated by the foregoing conventional method, the electron mobility is restricted due to photoresist and chemicals residues left on the polysilicon layer 104, as shown in Figure 1B. In addition, other characteristics of the low temperature TFT, such as the value of the threshold voltage and the sub-threshold swing, can be affected by the presence of photoresist and chemicals residues remaining in the device.

SUMMARY OF THE INVENTION

[0009] It is therefore an object of the invention to provide an improved method for fabricating a low temperature polysilicon thin film transistor without photoresist and chemicals residues.

[0010] The invention achieves the above-identified objects by providing a method for fabricating a NMOS transistor and a PMOS transistor on a substrate. The method includes the steps of: forming a buffer layer on the substrate; forming a polysilicon layer on the buffer layer, wherein the

polysilicon layer preferably has a thickness between about 200 angstroms and 1000 angstroms; forming a gate oxide layer on the polysilicon layer, wherein the gate oxide layer preferably has a thickness between about 500 angstroms and 1500 angstroms; forming a photoresist pattern on the gate oxide layer; etching the polysilicon layer and the gate oxide layer and using the photoresist pattern as a mask by photolithography to form a first stack structure corresponding to the NMOS transistor and to form a second stack structure corresponding to the PMOS transistor; removing the photoresist pattern; forming a gate on the gate oxide layer, wherein the gate includes molybdenum, chromium, or thallium/aluminum/thallium; forming source/drain region of the NMOS transistor by implanting first heavy dopants and using a photoresist layer covering the second stack structure and lightly doped region of the NMOS transistor as a mask, wherein the first heavy dopants include phosphorus with the preferred dosage between about 1E14 dose/cm^2 and 5E15 dose/cm^2; implanting dopants to form the lightly doped region of the NMOS transistor by using the gate as a mask, wherein the dopants include phosphorus with the preferred dosage between about 8E12 dose/cm^2 and 5E13 dose/cm^2; and implanting second heavy dopants to form source/drain region of the PMOS transistor by using a photoresist layer over the first stack structure as a mask, wherein the second heavy dopants include phosphorus with the preferred dosage between about 1E14 dose/cm^2 and 5E15

dose/cm2.

[0011] Embodiments of the invention further includes: forming an interlayer dielectric on the gate oxide layer, the gate and the substrate, wherein the interlayer dielectric preferably has a thickness between about 2000 angstroms and 7000 angstroms; selectively exposing the gate, the source/drain regions of the NMOS transistor and the PMOS transistor; forming a patterned passivation layer on the interlayer dielectric and the electrodes, wherein the patterned passivation layer exposes a portion of the electrodes of the NMOS transistor in a pixel area; and forming a transparent electrode to electrically connect the exposed portion of the electrodes of the NMOS transistor exposed, wherein the transparent electrode includes indium tin oxide (ITO).

[0012] Other objects, features, and advantages of the invention will become apparent from the following detailed description of the preferred but non-limiting embodiments. The following description is made with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Figures 1A to 1J (Prior Art) are cross-sectional views showing the sequential process steps of a conventional method for fabricating a low temperature polysilicon thin film transistor.

[0014] Figures 2A to 2J are cross-sectional views showing the sequential process steps of the method for fabricating a low temperature polysilicon thin film transistor in accordance with one preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0015] The present invention aims to provide an improved method for fabricating a low temperature polysilicon thin film transistor without residues of photoresist and chemicals.

[0016] Figures 2A to 2J are cross-sectional views showing the sequential process steps of the method for fabricating a low temperature polysilicon thin film transistor in accordance with one preferred embodiment of the present invention. Referring first to Figure 2A, a buffer layer 202 and a polysilicon layer 204 are sequentially formed on a substrate 200. The buffer layer 202 can be a silicon oxide layer or a silicon nitride layer, and the substrate 200 can be a glass substrate or a plastic substrate. The polysilicon layer 204 can be formed by annealing amorphous silicon using excimer laser. The polysilicon layer 204 can have a thickness between about 200 angstroms and 1000 angstroms.

[0017] Next, a gate oxide layer 208 is formed on the polysilicon layer 204.

The gate oxide layer 208 can be made of silicon dioxide, and can have a thickness between about 500 angstroms and 1500 angstroms. Then, a patterned photoresist layer 205 is formed on the polysilicon layer 204, and the gate oxide layer 208 and the polysilicon layer 204 are etched using the patterned photoresist layer 205 as a mask. The removal of the residues of the photoresist layer 205 on the gate oxide layer 208 is performed by using chemicals, such as wet dip. The structure after wet dip is shown in Figure 2B. In Figure 2B, there are three stack structures having the gate oxide layer 208 and the polysilicon layer 204. The middle and the left ones respectively function as the NMOS device and the PMOS device of the CMOS transistor. The stack structure on the right of the three stack structures is the NMOS device in the pixel area.

[0018] Compared with the conventional manufacturing process, the manufacturing process of the invention has no step between the formation of the polysilicon layer 204 and the gate oxide layer 208. The conventional process includes steps such as forming the photoresist layer 105 on the polysilicon layer 104 and removing the photoresist layer 105 by using chemicals, which do not exist in the method of the present invention. Thus, the problem of photoresist and chemical residues between the gate oxide layer 208 and the polysilicon layer 204 is overcome by applying the process

of this invention. This improvement further benefits the quality of the low temperature polysilicon TFTs.

[0019] Referring to Figure 2C, a conductive layer is disposed on the gate oxide layer 208. Photolithography and etching processes are then performed to define the patterned conductive layer and form a gate 210. The material of the gate 210 can be molybdenum (Mo), chromium (Cr), thallium/aluminum/thallium (Ti/Al/Ti) or their combination. Next, referring to Figure 2D, a patterned photoresist layer 212 is formed on the gate 210 and on the gate oxide layer 208. Then, a heavily doping process, using high dosage of phosphorus, is performed to form source/drain regions 204a, 204b, 204c, 204d of a NMOS transistor. The dosage of phosphorus implanted can be between about 1E14 dose/cm^2 and 5E15 dose/cm^2.

[0020] The photoresist layer 212 then is removed. Low dosage of phosphorus is then implanted into the substrate 200 to form a lightly doped source/drain regions 104m, 104n, 104x, 104y of the NMOS transistor, as shown in Figure 2E. The dosage of phosphorus implanted is between about 8E12 dose/cm^2 and 5E13 dose/cm^2. Next, referring to Figure 2F, a photoresist layer 214 is formed over the substrate 200 on the gate 210 and the gate oxide layer 208. Using the photoresist layer 214 as a mask, high dosage of boron is implanted in the substrate 200 to form source/drain region

204i, 204j of a PMOS transistor. The dosage of boron implanted is between about 1E14 dose/cm^2 and 5E15 dose/cm^2.

[0021] Referring to Figure 2G, the photoresist layer 214 is removed. An interlayer dielectric 216 is formed on the gate 210 and on the gate oxide layer 208. There are a number of openings formed within the gate oxide layer 208 and within the interlayer dielectric 216 thereon. The interlayer dielectric 216 can be made of silicon dioxide, and can have a thickness between about 2000 angstroms and 7000 angstroms. Then, referring to Figure 2H, a conductive layer, filling the openings within the gate oxide layer 208 and the interlayer dielectric 116, is formed on the interlayer dielectric 216. The conductive layer forms electrodes 218 electrically connecting the gate 210, the source/drain regions 204a, 204c, 204i, 204b, 204d and 204j.

[0022] Referring to Figure 2I, a passivation layer 220 is formed on the electrodes 218 and on the interlayer dielectric 216. An opening formed within the passivation layer 220 exposes a part of the electrodes 218. Next, a transparent electrode 222 is formed on the passivation layer 220 and fills in the opening through the passivation layer 220 to electrically connect the electrode 218, as shown in Figure 2J. The transparent electrode 222 can be made of a conductive transparent material such as indium tin oxide (ITO).

[0023] With the abovementioned manufacturing process, the residues of photoresist and chemicals on the polysilicon layer 204 can be effectively prevented. The electron mobility of the low temperature polysilicon TFT is improved as a result of the improved smooth interface between the polysilicon layer 204 and the gate oxide layer 208. Some other defects occurring on the devices manufactured by the conventional method, such as abnormal shifting of the threshold voltage and sub-threshold swing, are effectively prevented.

[0024] While the invention has been described by way of example and in terms of a preferred embodiment, it is to be understood that the invention is not limited thereto. On the contrary, it is intended to cover various modifications and similar arrangements and procedures, and the scope of the appended claims therefore should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements and procedures.